Amendments to the Claims

The following listing of claims will replace all prior versions, and listings, of claims in the present application:

1. (canceled)

2. (original) A multiple die semiconductor assembly comprising:

a first semiconductor die defining a first active surface, said first active surface including at least one conductive bond pad;

a second semiconductor die defining a second active surface, said second active surface including at least one conductive bond pad;

an intermediate substrate positioned between said first semiconductor die and said second semiconductor die such that a first surface of said intermediate substrate faces said first semiconductor die and such that a second surface of said intermediate substrate faces said second semiconductor die, wherein

said intermediate substrate defines a passage there through, and

one of said first semiconductor die and said second semiconductor die is positioned such that said conductive bond pad on one of said first and second active surfaces is aligned with said passage; and

at least one decoupling capacitor conductively coupled to at least one of said first and second semiconductor dies, wherein a thickness dimension of said decoupling capacitor is accommodated in a space defined by a thickness dimension of one of

said first semiconductor die,

said second semiconductor die,

a topographic contact conductively coupled to said first semiconductor die, and

a topographic contact conductively coupled to said second semiconductor die.

3. (canceled)

4. (canceled)

5. (currently amended) A multiple die semiconductor assembly comprising:

a first semiconductor die defining a first active surface, said first active surface including at least one conductive bond pad;

a second semiconductor die defining a second active surface, said second active surface including at least one conductive bond pad;

an intermediate substrate positioned between said second semiconductor die and said first active surface of said first semiconductor die such that a first surface of said intermediate substrate faces said first active surface and such that a second surface of said intermediate substrate faces said second semiconductor die, wherein

said intermediate substrate includes a network of conductive contacts formed thereon,

said intermediate substrate defines a passage there through,

said first semiconductor die is secured to said first surface of said intermediate substrate such that said conductive bond pad of said first semiconductor die is aligned with said passage, and

said first semiconductor die is electrically coupled to said intermediate substrate by at least one conductive line extending from said conductive bond pad of said first semiconductor die through said passage defined in said intermediate substrate and to a conductive contact on said second surface of said intermediate substrate; and

an additional substrate positioned such that a first surface of said additional substrate faces said second active surface of said second semiconductor die and such that said first surface of said additional substrate opposes said second surface of said intermediate substrate, wherein

said additional substrate includes a network of conductive contacts formed thereon,

said additional substrate defines an additional passage there through,

said second semiconductor die is secured to said first surface of said additional substrate such that said conductive bond pad of said second semiconductor die is aligned with said additional passage, and

said second semiconductor die is electrically coupled to said additional substrate by at least one conductive line extending from said conductive bond pad of said second semiconductor die through said additional passage defined in said additional substrate and to a conductive contact on a second surface of said additional substrate.

6. (original) A multiple die semiconductor assembly comprising:

a first semiconductor die defining a first active surface, said first active surface including at least one conductive bond pad;

a second semiconductor die defining a second active surface, said second active surface including at least one conductive bond pad;

an intermediate substrate positioned between said first active surface of said first semiconductor die and said second active surface of said second semiconductor die such that a first surface of said intermediate substrate faces said first active surface and such that a second surface of said intermediate substrate faces said second active surface, wherein

said first semiconductor die is electrically coupled to said intermediate substrate by at least one topographic contact extending from said first active surface to said first surface of said intermediate substrate,

said intermediate substrate defines a passage there through,

said second semiconductor die is secured to said second surface of said intermediate substrate such that said conductive bond pad of said second semiconductor die is aligned with said passage, and

said second semiconductor die is electrically coupled to said intermediate substrate by at least one conductive line extending from said conductive bond pad of said second semiconductor die through said passage defined in said

intermediate substrate and to a conductive contact on said first surface of said intermediate substrate; and

at least one decoupling capacitor conductively coupled to at least one of said first and second semiconductor dies, wherein a thickness dimension of said decoupling capacitor is accommodated in a space defined by a thickness dimension of one of

said first semiconductor die,

said second semiconductor die,

a topographic contact conductively coupled to said first semiconductor die, and

a topographic contact conductively coupled to said second semiconductor die.

7. (original) A multiple die semiconductor assembly comprising:

a first semiconductor die defining a first active surface, said first active surface including at least one conductive bond pad;

a second semiconductor die defining a second active surface, said second active surface including at least one conductive bond pad;

an intermediate substrate positioned between said second semiconductor die and said first active surface of said first semiconductor die such that a first surface of said intermediate substrate faces said first active surface and such that a second surface of said intermediate substrate faces said second semiconductor die, wherein

said intermediate substrate defines a passage there through,

said first semiconductor die is secured to said first surface of said intermediate substrate such that said conductive bond pad of said first semiconductor die is aligned with said passage, and

said first semiconductor die is electrically coupled to said intermediate substrate by at least one conductive line extending from said conductive bond pad of said first semiconductor die through said passage defined in said intermediate substrate and to a conductive contact on said second surface of said intermediate substrate;

an additional substrate positioned such that a first surface of said additional substrate faces said second active surface of said second semiconductor die, wherein

said additional substrate defines an additional passage there through,

said second semiconductor die is secured to said first surface of said additional substrate such that said conductive bond pad of said second semiconductor die is aligned with said additional passage, and

said second semiconductor die is electrically coupled to said additional substrate by at least one conductive line extending from said conductive bond pad of said second semiconductor die through said additional passage defined in said additional substrate and to a conductive contact on a second surface of said additional substrate; and

at least one decoupling capacitor conductively coupled to at least one of said first and second semiconductor dies, wherein a thickness dimension of said decoupling capacitor is accommodated in a space defined by a thickness dimension of one of

said first semiconductor die,

said second semiconductor die,

a topographic contact conductively coupled to said first semiconductor die, and

a topographic contact conductively coupled to said second semiconductor die.

8. (currently amended) A multiple die semiconductor assembly comprising:

a first semiconductor die defining a first active surface, said first active surface including at least one conductive bond pad;

a second semiconductor die defining a second active surface, said second active surface including at least one conductive bond pad; and

an intermediate substrate positioned between said first active surface of said first semiconductor die and said second active surface of said second semiconductor die such that a first surface of said intermediate substrate faces said first active surface and such that a second surface of said intermediate substrate faces said second active surface, wherein

said intermediate substrate includes a network of conductive contacts formed thereon,

said first semiconductor die is electrically coupled to said intermediate substrate by at least one topographic contact extending from said first active surface to said first surface of said intermediate substrate, and

said second semiconductor die is electrically coupled to said intermediate substrate by at least one topographic contact extending from said second active surface to said second surface of said intermediate substrate.

9. (original) A multiple die semiconductor assembly as claimed in claim 8 wherein said assembly further comprises at least one decoupling capacitor conductively coupled to at least one of said first and second semiconductor dies, wherein a thickness dimension of said decoupling capacitor is accommodated in a space defined by a thickness dimension of said topographic contact extending from said first active surface to said first surface of said intermediate substrate.

10-24. (canceled)

25. (currently amended) A multiple die semiconductor assembly as claimed in claim 2 ~~claim 1~~ wherein said first semiconductor die comprises a flip chip arranged relative to said intermediate substrate such that said conductive bond pads included in said first active surface are aligned with conductive contacts on said first surface of said intermediate substrate.

26. (original) A multiple die semiconductor assembly as claimed in claim 25 wherein said multiple die semiconductor assembly further comprises topographic contacts extending between said conductive bond pads of said first active surface and said conductive contacts of said first surface of said intermediate substrate.

27. (currently amended) A multiple die semiconductor assembly as claimed in claim 2 ~~claim 1~~ wherein said second semiconductor die comprises a flip chip arranged relative to said

intermediate substrate such that said conductive bond pads included in said second active surface are aligned with a conductive contact on said second surface of said intermediate substrate.

28. (original) A multiple die semiconductor assembly as claimed in claim 27 wherein said multiple die semiconductor assembly further comprises topographic contacts extending between said conductive bond pads of said second active surface and said conductive contacts of said second surface of said intermediate substrate.

29. (currently amended) A multiple die semiconductor assembly as claimed in claim 2 ~~claim 1~~ wherein said first semiconductor die comprises a stacked chip secured to said first surface of said intermediate substrate such that said conductive bond pads on said first active surface are aligned with said passage.

30. (original) A multiple die semiconductor assembly as claimed in claim 29 wherein said multiple die semiconductor assembly further comprises conductive lines extending from said conductive bond pads on said first active surface to conductive contacts on said second surface of said intermediate substrate.

31. (currently amended) A multiple die semiconductor assembly as claimed in claim 2 ~~claim 1~~ wherein said second semiconductor die comprises a stacked chip secured to said second surface of said intermediate substrate such that said conductive bond pad on said second active surface is aligned with said passage.

32. (original) A multiple die semiconductor assembly as claimed in claim 31 wherein said multiple die semiconductor assembly further comprises conductive lines extending from said conductive bond pads on said second active surface to conductive contacts on said first surface of said intermediate substrate.

33. (currently amended) A multiple die semiconductor assembly as claimed in claim 2 ~~claim 1~~ wherein:

said first semiconductor die is electrically coupled to said intermediate substrate; and said second semiconductor die is electrically coupled to said intermediate substrate.

34. (currently amended) A multiple die semiconductor assembly as claimed in claim 2 ~~claim 1~~ wherein said first semiconductor die is electrically coupled to said second semiconductor die.

35. (currently amended) A multiple die semiconductor assembly as claimed in claim 2 ~~claim 1~~ wherein:

said first semiconductor die is electrically coupled to said intermediate substrate by at least one conductive line extending from said conductive bond pad of said first semiconductor die through said passage defined in said intermediate substrate and to said second surface of said intermediate substrate.

36. (currently amended) A multiple die semiconductor assembly as claimed in claim 2 ~~claim 1~~ wherein:

said second semiconductor die is electrically coupled to said intermediate substrate by at least one conductive line extending from said conductive bond pad of said second semiconductor die through said passage defined in said intermediate substrate and to said first surface of said intermediate substrate.

37. (currently amended) A multiple die semiconductor assembly as claimed in claim 2 ~~claim 1~~ wherein said assembly further comprises an underfill material formed over said first surface of said intermediate substrate.

38. (currently amended) A multiple die semiconductor assembly as claimed in claim 2 ~~claim 1~~ wherein said assembly further comprises an underfill material formed between said first semiconductor die and said first surface of said intermediate substrate.

39. (currently amended) A multiple die semiconductor assembly as claimed in claim 2 ~~claim 1~~ wherein said assembly further comprises an encapsulant formed over said first semiconductor die and said first surface of said intermediate substrate.

40. (original) A multiple die semiconductor assembly as claimed in claim 39 wherein said assembly further comprises an underfill material formed between said first semiconductor die and said first surface of said intermediate substrate.

41. (currently amended) A multiple die semiconductor assembly as claimed in claim 2 ~~claim 1~~ wherein said assembly further comprises an encapsulant formed over said first semiconductor die and said first surface of said intermediate substrate and between said first semiconductor die and said first surface of said intermediate substrate.

42. (currently amended) A multiple die semiconductor assembly as claimed in claim 2 ~~claim 1~~ wherein said assembly further comprises an encapsulant formed over said second semiconductor die.

43. (currently amended) A multiple die semiconductor assembly as claimed in claim 2 ~~claim 1~~ wherein said assembly further comprises a die attach adhesive positioned to secure said second semiconductor die to said second surface of said intermediate substrate.

44. (canceled)

45. (original) A multiple die semiconductor assembly as claimed in claim 6 wherein:

said decoupling capacitor is mounted to said first surface of said intermediate substrate; and

the thickness dimension of said decoupling capacitor is accommodated in a space defined by a thickness dimension of a topographic contact conductively coupled to a conductive contact on said first surface of said intermediate substrate.

46. (original) A multiple die semiconductor assembly as claimed in claim 45 wherein the thickness dimension of said decoupling capacitor is accommodated in a space further defined by a thickness dimension of said first semiconductor die.

47. (original) A multiple die semiconductor assembly as claimed in claim 6 wherein:

said assembly comprises a pair of decoupling capacitors mounted to said first surface of said intermediate substrate; and

said first semiconductor die is positioned between said pair of decoupling capacitors relative to said first surface of said intermediate substrate.

48. (original) A multiple die semiconductor assembly as claimed in claim 6 wherein:

said decoupling capacitor is mounted to said first surface of said intermediate substrate; and

the thickness dimension of said decoupling capacitor is accommodated in a space defined by a thickness dimension of said first semiconductor die conductively coupled to said first surface of said intermediate substrate.

49. (original) A multiple die semiconductor assembly as claimed in claim 7 wherein:

said assembly further comprises a third substrate positioned such that a first surface of said third substrate faces said second surface of said additional substrate;

said additional substrate is electrically coupled to said third substrate by at least one topographic contact extending from said second surface of said additional substrate to a first surface of said third substrate;

said decoupling capacitor is mounted to said first surface of said third substrate; and

the thickness dimension of said decoupling capacitor is accommodated in a space defined by a thickness dimension of said topographic contact extending from said second surface of said additional substrate to a first surface of said third substrate.

50. (original) A multiple die semiconductor assembly as claimed in claim 7 wherein:

said assembly further comprises a third substrate positioned such that a first surface of said intermediate substrate faces a second surface of said third substrate;

said intermediate substrate is electrically coupled to said third substrate by at least one topographic contact extending from said second surface of said third substrate to said first surface of said intermediate substrate;

said decoupling capacitor is mounted to said second surface of said third substrate; and

the thickness dimension of said decoupling capacitor is accommodated in a space defined by a thickness dimension of said topographic contact extending from said second surface of said third substrate to said first surface of said intermediate substrate.

51. (original) A multiple die semiconductor assembly as claimed in claim 50 wherein the thickness dimension of said decoupling capacitor and a thickness dimension of said first semiconductor die are both accommodated in said space defined by the thickness dimension of said topographic contact extending from said second surface of said third substrate to said first surface of said intermediate substrate.

52. (original) A multiple die semiconductor assembly as claimed in claim 7 wherein:

said decoupling capacitor is mounted to said first surface of said intermediate substrate; and

the thickness dimension of said decoupling capacitor is accommodated in a space defined by a thickness dimension of said first semiconductor die.

53. (original) A multiple die semiconductor assembly as claimed in claim 52 wherein:

said assembly comprises a pair of decoupling capacitors mounted to said first surface of said intermediate substrate; and

said first semiconductor die is positioned between said pair of decoupling capacitors relative to said first surface of said intermediate substrate.

54. (new) A multiple die semiconductor assembly as claimed in claim 2 wherein said intermediate substrate includes a network of conductive contacts formed thereon.

55. (new) A multiple die semiconductor assembly as claimed in claim 6 wherein said intermediate substrate includes a network of conductive contacts formed thereon.

56. (new) A multiple die semiconductor assembly as claimed in claim 7 wherein said intermediate substrate includes a network of conductive contacts formed thereon.

57. (new) A multiple die semiconductor assembly comprising:

a first semiconductor die defining a first active surface, said first active surface including at least one conductive bond pad;

a second semiconductor die defining a second active surface, said second active surface including at least one conductive bond pad;

an intermediate substrate positioned between said first semiconductor die and said second semiconductor die such that a first surface of said intermediate substrate faces said first semiconductor die and such that a second surface of said intermediate substrate faces said second semiconductor die, wherein

said intermediate substrate defines a passage there through, and

one of said first semiconductor die and said second semiconductor die is positioned such that said conductive bond pad on one of said first and second active surfaces is aligned with said passage; and

at least one decoupling capacitor conductively coupled to at least one of said first and second semiconductor dies, wherein a thickness dimension of said decoupling capacitor is accommodated in a space defined by a thickness dimension of a topographic contact conductively coupled to said first semiconductor die or said second semiconductor die.

58. (withdrawn - new) A multiple die semiconductor assembly as claimed in claim 2 further comprising a heat sink comprising a cap portion and a peripheral portion, wherein:

said cap portion is thermally coupled to a major surface of at least one of said first and second semiconductor dies; and

said peripheral portion engages a mounting zone defined by a lateral dimension of said intermediate substrate extending beyond a periphery of at least one of said first and second semiconductor dies.

59. (withdrawn - new) A multiple die semiconductor assembly as claimed in claim 5 further comprising a heat sink comprising a cap portion and a peripheral portion, wherein:

said cap portion is thermally coupled to a major surface of at least one of said first and second semiconductor dies; and

said peripheral portion engages a mounting zone defined by a lateral dimension of said intermediate substrate extending beyond a periphery of at least one of said first and second semiconductor dies.

60. (withdrawn - new) A multiple die semiconductor assembly as claimed in claim 6 further comprising a heat sink comprising a cap portion and a peripheral portion, wherein:

said cap portion is thermally coupled to a major surface of at least one of said first and second semiconductor dies; and

said peripheral portion engages a mounting zone defined by a lateral dimension of said intermediate substrate extending beyond a periphery of at least one of said first and second semiconductor dies.

61. (withdrawn - new) A multiple die semiconductor assembly as claimed in claim 7 further comprising a heat sink comprising a cap portion and a peripheral portion, wherein:

said cap portion is thermally coupled to a major surface of at least one of said first and second semiconductor dies; and

said peripheral portion engages a mounting zone defined by a lateral dimension of said intermediate substrate extending beyond a periphery of at least one of said first and second semiconductor dies.

62. (withdrawn - new) A multiple die semiconductor assembly as claimed in claim 8 further comprising a heat sink comprising a cap portion and a peripheral portion, wherein:

said cap portion is thermally coupled to a major surface of at least one of said first and second semiconductor dies; and

said peripheral portion engages a mounting zone defined by a lateral dimension of said intermediate substrate extending beyond a periphery of at least one of said first and second semiconductor dies.